REMARKS

In the present application, claims 1-33 are pending. Claims 1-33 are rejected. Claims 1, 14, 15, 17, 18, 25, and 32 have been amended. No new matter has been added. As a result of this response, claims 1-33 are believed to be in condition for allowance.

Claim Rejections – 35 USC § 112

The Examiner rejected claims 16 and 33 as being indefinite for failing to particularly point and distinctly claim the subject matter of the invention. Specifically, the Examiner states that it is "not understood how the circuit can be operated with a supply voltage of about one volt, where the supply voltage comes from and how this voltage can be connected to the circuit."

Applicants respectfully reply that the supply voltage, V_{DD}, is discussed at length throughout the specification, for example in reference to Fig. 8B, wherein there is detailed a physical point of introduction for the supply voltage. The specification is similarly directed, as a whole, to describing "how the circuit can be operated". Lastly, it is commonly known in the art of circuit design and construction that it is possible to obtain a voltage supply. Claim 16 is amended herein to make clear that the method comprises "coupling M_1, M_2 and M_B to a supply voltage". As a result, Applicants respectfully traverse the Examiner's grounds for rejection.

Claim Rejections – 35 USC § 103

The Examiner rejected claims 1-33 as being unpatentable over Figures 1, 5A, and 7A of the Applicant's admitted prior art in view of Tsuchi (US2002/0084840). The Examiner asserted that the admitted prior art discloses a first and second input device each having a control terminal coupled to a radio frequency input signal, and a bias setting device having a control terminal coupled to the radio frequency input signal and an output coupled to the control terminal of each input device. The Examiner further notes, "However, the admitted prior art does not disclose that the transistors [sic] is partitioned into two equal sized paralleled bias setting devices" where the bias setting devices are coupled to the control terminals of the input devices for establishing a bias voltage at the control terminals. The Examiner further asserts that Tsuchi teaches "a circuit comprising a transistor ... being replaced by two parallel transistors ... having the same size for preventing a variance in transistor characteristics caused by the manufacturing process". Lastly, the Examiner asserts that "It would have been obvious ... to employ two equal size biasing

transistors as taught by Tsuchi in the circuits of the admitted prior art for the purpose of preventing a variance of the transistors characteristics caused by the manufacturing process." The Examiner then asserts that "Noted [sic] that the modified circuits of the admitted prior art in view of Tsuchi would provide circuits having structures similar to the claimed structures as recited in claims 2-9, 17-21, and 29-32.

Applicants respectfully disagree the Examiner's assertions. Specifically, combining the teachings of Tsuchi with that of the admitted prior art, such a combination neither being suggested nor deemed proper, may render the resulting circuit inoperable. In addition, such a combination would fail to teach at least one element of the invention as claimed.

With reference to claim 1, there is recited:

1. A transconductor circuit, comprising:

a first input device M_1 and a second input device M_2 each having a control terminal coupled to a **differential radio frequency input signal**; and

a bias setting device M_B having a control terminal coupled to **said differential radio frequency input signal** and an output coupled to said control terminal of each of said M_1 and M_2, where M_B is partitioned into two equal sized paralleled bias setting devices M_{B1} and M_{B2}, where **M_{B1} and M_{B2} are coupled to said control terminals of M_1 and M_2 for establishing a bias voltage at the control terminals of M_1 and M_2** and wherein said differential radio frequency input signal is coupled to a base of M_{B1} and a base of M_{B2}. (emphasis added)

As the MPEP states at §2143.01, "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)." Claim 1 has been amended to more precisely recite that the radio frequency input signal is a differential signal. Support for this clarification may be found in the specification at least at page 10, lines 11-15. As a result of this clarification, it is evident that the combination suggested by the Examiner would result in a circuit both lacking the elements of recited in claim 1 and incapable of performing its intended purpose.

Specifically, a differential signal, such as the claimed "differential radio frequency input signal" is comprised of two signals. Claim 1 makes explicit the presence of a first and second input device (M_1 and M_2) for accepting the differential radio frequency input signal. Claim 1 likewise explicitly recites that the bias setting device is coupled to the differential radio frequency input signal and that the outputs of the paralleled bias setting devices (created by partitioning the bias setting device) are coupled to the control terminals of the two input devices.

In contrast to the Examiner's assertions, employing "two equal size biasing transistors as taught by Tsuchi" to the single transistor of the admitted prior art would not result in "circuits having structures similar to the claimed structures". In fact, the result would be inoperable for the following reasons. Referring specifically to the Examiner's citation, while Tsuchi does teach at Figure 12 and page 12, col. 1, lines 13-22, replacing transistor 211 with two parallel transistors 211A and 211B, such a configuration cannot be made to work with the differential input signal as claimed. Claim 1 has been amended to make clear that the bases (or gates) of each transistor, M_{B1} and M_{B2}, are coupled to the differential input signal. A differential signal is formed of two differential, or balanced signals. As Fig. 8b makes clear, the differential signal formed of V_{RF+} and V_{RF-} is coupled such that V_{RF+} is coupled to the base of M_{B1} and V_{RF-} is coupled to the base of M_{B2}.

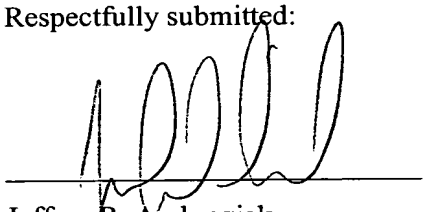
In contrast, Tsuchi teaches the replacement of a single transistor having a single-ended input which is not coupled to a base of the transistor, with two parallel transistors having a single-ended input which is not coupled to either base of either of the two parallel transistors. Specifically, the parallel transistors 211A and 211B substituted for transistor 211 in Fig. 12 function in concert to provide the same functionality as transistor 211 while perhaps resulting in less manufacturing variance. The inputs and outputs of the parallel transistors, 211A and 211B, do not change. Both transistor 211A and 211B receive the same single-ended input, and, it should be noted, the input signal V_{in} is not connected to the bases of 211A and 211B as recited in claim 1. As noted above, the claimed "equal sized paralleled bias setting devices M_{B1} and M_{B2}" receive as input the "differential radio frequency input signal". As a result, applying the teachings of Tsuchi to the admitted prior art would result in a circuit topology requiring a single-ended input. Such a topology is inoperable when the input signal is formed of a differential signal as claimed.

As a result, the Examiner's rejection of claim 1 is therefore traversed. As claims 2-13 depend upon claim 1, claims 2-13 are likewise in condition for allowance. Both independent claims 15 and 28 make similar reference to the elements discussed with reference to claim 1. Therefore, claims 15 & 28, are likewise in condition for allowance. As claims 16-27 and 29-33 depend on claims 15 and 28, they are likewise in condition for allowance.

An earnest and thorough attempt has been made by the undersigned to resolve the outstanding issues in this case and place same in condition for allowance. If the Examiner has any questions or feels that a telephone or personal interview would be helpful in resolving any outstanding issues which remain in this application after consideration of this amendment, the Examiner is courteously invited to telephone the undersigned and the same would be gratefully appreciated.

It is submitted that the claims herein patentably define over the art relied on by the Examiner and early allowance of same is courteously solicited.

Respectfully submitted:



7 June 05

Jeffrey R. Ambroziak — Date

Reg. No.: 47,387

Customer No.: 29683

HARRINGTON & SMITH, LLP
4 Research Drive
Shelton, CT 06484-6212

Telephone: (203)925-9400
Facsimile: (203)944-0245
email: jambroziak@hspatent.com

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450.

6-7-05 Claire F. Musser

Date Name of Person Making Deposit